Electronic Version
Stylesheet Version v1.1.1

MULTIPROCESSOR CODE FIX USING A LOCAL CACHE

Abstract

Operating code fixes are supplied to multiple processors utilizing the same operating code by storing the correction code fixes in a central RAM, and distributing the code fixes over a dedicated code fix bus to a local cache for each processor. The first processor encountering a code fix requests the code fix from the RAM, which then distributes the code fix over the code fix bus to all of the local caches which are automatically updated with the new code. The system is particularly applicable to an integrated circuit having multiple processors fabricated on a chip, wherein the RAM is on-chip and is connected to an off-chip EEPROM that loads corrected code fixes to the on-chip RAM at power-up.